151. (Amended) A method of operation of a synchronous memory device, wherein the memory device includes an array of memory cells, the method of operation comprises:

receiving an external clock signal;

receiving block size information, wherein the block size information defines an amount of data to be output by the memory device in response to a first operation code;

receiving the first operation code synchronously with respect to the external clock signal wherein the first operation code instructs the memory device to perform a read operation; and

outputting the amount of data in response to the first operation code.

152. (Amended) The method of claim 151 wherein the block size information also defines an amount of data to be input by the memory device, wherein the amount of data is input in response to a second operation code, and wherein the second operation code instructs the memory device to perform a write operation, the method further including:

receiving the second operation code synchronously with respect to a transition of the external clock signal; and

inputting the amount of data in response to the second operation code.

153. (Amended) The method of claim 152 wherein a first portion of the amount of data is sampled, in response to the second operation code, after a delay time transpires.

154. The method of claim 151 wherein the amount of data is output synchronously with respect to the external clock signal.

155. (Amended) The method of claim 154 wherein a first portion of the amount of data is output synchronously with respect to a rising edge transition of the external clock signal and a second portion of the amount of data is output synchronously with respect to a falling edge transition of the external clock signal.

156. (Amended) The method of claim 151 wherein the memory device receives the block size information synchronously with respect to the external clock signal.

157. (Amended) The method of claim 151 wherein the first operation code includes precharge information.

158. (Amended) The method of claim 151 wherein the first operation code is included in a request packet.

159. (Amended) The method of claim 158 wherein the block size information and the first operation code are both included in the same request packet.

160. The method of claim 158 wherein the request packet includes address information.

161. (Amended) The method of claim 151 wherein the block size information is an encoded value and wherein the block size information is sampled synchronously with respect to a rising or falling edge of the external clock signal.

162. (Amended) The method of claim 151 further including:

receiving a value which is representative of a number of clock cycles of the external clock signal to transpire before the memory device outputs the data; and

receiving a third operation code wherein the third operation code instructs the memory device to store the value in a programmable register on the memory device.

163. (Amended) The method of claim 162 wherein the memory device outputs the data on an external bus after the number of clock cycles of the external clock signal transpire.

14 164. (Amended) The method of claim 12 wherein the external bus includes a plurality of signal lines to multiplex control information, address information, and the amount of data.

15 165. (Amended) A method of controlling a synchronous memory device by a controller, wherein the memory device includes an array of memory cells, the method of controlling the memory device comprises:

providing block size information to the memory device synchronously with respect to an external clock signal, wherein the block size information defines an amount of data to be output by the memory device; and

issuing a first operation code to the memory device synchronously with respect to the external clock signal, wherein the first operation code instructs the memory device to perform a read operation.

16 166. The method of claim 15 further including receiving the amount of data from the memory device.

17 167. (Amended) The method of claim 15 further including providing a binary value to the memory device, wherein the binary value is representative of a number of clock cycles of the external clock signal to transpire before the memory device outputs the amount of data in response to the first operation code.

18 168. (Amended) The method of claim 17 further including providing a second operation code to the memory device, wherein the second operation code instructs the memory device to store the binary value in a register on the memory device.

19 169. (Amended) The method of claim 15 wherein the first operation code is issued synchronously with respect to a rising or falling edge transition of the external clock signal.

20 170. (Amended) The method of claim 15 wherein the first operation code includes precharge information.

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171. (Amended) The method of claim 163 wherein the first operation code is provided to the memory device via an external bus.

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172. (Amended) The method of claim 171 wherein the external bus includes a plurality of signal lines to multiplex control information, address information and data.

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173. (Amended) The method of claim 165 wherein the block size information and the first operation code are both included in a request packet.

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174. (Amended) The method of claim 163 further including providing address information to the memory device.

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175. The method of claim 165 wherein the block size information is a binary code.

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176. (Amended) A synchronous dynamic random access memory device having at least one memory section including a plurality of memory cells, the memory device comprising:

clock receiver circuitry to receive an external clock signal;

input receiver circuitry, including a first plurality of input receivers to receive block size information synchronously with respect to the external clock signal, wherein the block size information defines an amount of data to be output by the memory device in response to a first operation code; and

a plurality of output drivers to output the amount of data in response to the first operation code.

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177. The memory device of claim 176 wherein the amount of data is output synchronously with respect to the external clock signal.

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178. (Amended) The memory device of claim 177 wherein a first portion of the amount of data is output synchronously with respect to a rising edge transition of the external clock signal and a second

portion of the amount of data is output synchronously with respect to a falling edge transition of the external clock signal.

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179. (Amended) The memory device of claim 176 wherein the input receiver circuitry receives the first operation code synchronously with respect to the external clock signal.

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180. (Amended) The memory device of claim 179 wherein the input receiver circuitry includes a second plurality of input receivers to receive the first operation code.

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181. (Amended) The memory device of claim 180 wherein the first and second plurality of input receivers are coupled to an external bus.

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182. (Amended) The memory device of claim 181 wherein the external bus includes a plurality of signal lines to multiplex control information, address information and the data.

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183. (Amended) The memory device of claim 179 wherein the first operation code includes precharge information.

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184. (Amended) The memory device of claim 176 further including a programmable register to store a value which is representative of a number of clock cycles of the external clock signal to transpire before the memory device outputs the data in response to the first operation code.

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185. (Amended) The memory device of claim 176 wherein the block size information further defines an amount of data to be input by the memory device in response to a second operation code, wherein the second operation code instructs the memory device to perform a write operation, and wherein the input receiver circuitry receives the amount of data in response to the second operation code.

186. (Amended) The memory device of claim 185 wherein the input receiver circuitry and the plurality of output drivers are coupled to an external bus.

187. (Amended) The memory device of claim 186 wherein the external bus includes a plurality of signal lines to multiplex control information, address information and the amount of data to be input.

188. The memory device of claim 176 further including delay lock loop circuitry coupled to the clock receiver circuitry to generate an internal clock signal, wherein the plurality of output drivers output data in response to the internal clock signal.

189. (Amended) The method of claim 176 wherein the block size information is a binary code.